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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/806,073	03/22/2004	Jacques Majos	5310-05700	1394	
7590 12/16/2005			EXAMINER		
Eric B. Meyer		CHANG, JOSEPH			
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398			ART UNIT	PAPER NUMBER	
AUSTIN, TX	78767-0398	2817			

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applicat	Application No. Applicant(s)					
		10/806,0	73	MAJOS, JACQUES				
Office Action Summary			r	Art Unit				
		Joseph C	-	2817				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE MAIL asions of time may be available under the provisions of 37 SIX (6) MONTHS from the mailing date of this community of period for reply is specified above, the maximum statutor re to reply within the set or extended period for reply will, reply received by the Office later than three months after the patent term adjustment. See 37 CFR 1.704(b).	ING DATE OF T 7 CFR 1.136(a). In no evation. ry period will apply and v by statute, cause the ap	HIS COMMUNICATION rent, however, may a reply be tir rill expire SIX (6) MONTHS from plication to become ABANDONE	N. nely filed the mailing date of this c D (35 U.S.C. § 133).	•			
Status								
1)□	Responsive to communication(s) filed o	ın						
	This action is <b>FINAL</b> . 2b) This action is non-final.							
′=	3) Since this application is in condition for allowance except for formal matters, prosecution as to the mer							
-,	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Dispositi	on of Claims	·	,					
4)⊠	4)⊠ Claim(s) <u>1-6</u> is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
	Claim(s) is/are allowed.							
-	Claim(s) 1-6 is/are rejected.							
	Claim(s) is/are objected to.							
· ·	Claim(s) are subject to restriction	and/or election	equirement.					
	on Papers		·					
	•	vaminor						
9) The specification is objected to by the Examiner.								
10) The drawing(s) filed on 22 March 2004 is/are: a) accepted or b) objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority ι	ınder 35 U.S.C. § 119							
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:								
	<ol> <li>Certified copies of the priority documents have been received.</li> <li>Certified copies of the priority documents have been received in Application No</li> </ol>							
	3. Copies of the certified copies of the priority documents have been received in this National Stage							
	application from the International Bureau (PCT Rule 17.2(a)).							
* See the attached detailed Office action for a list of the certified copies not received.								
Attachmen	t(s)							
	e of References Cited (PTO-892)	(PTO-413)						
	e of Draftsperson's Patent Drawing Review (PTO-		Paper No(s)/Mail Da	Mail Date mal Patent Application (PTO-152)				
	nation Disclosure Statement(s) (PTO-1449 or PTC r No(s)/Mail Date	(00)14610	6) Other:	atom application (FTC	J 192;			

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#### **DETAILED ACTION**

## Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Majos Jacques, EP1187308 in view of Yu et al., US Patent 5793096 for reasons of record.

Regarding the amended recitation "thereby allowing the inductor chip area to be reduced as a function of the mutual inductance coefficient of the stacked inductors", the functional limitation as recited inherently present in the modified structure of the combined prior arts, and therefore it still would have been obvious to one of ordinary skill in the art to recognized that two inductors be superposed one on top op the other because such a modification would have provided the benefit of further reducing the chip area as stated in the previous Office Action.

### **Response to Arguments**

Applicant's arguments filed 10/7/05 have been fully considered but they are not persuasive.

Regarding applicant comments directed to the rejection of claims 1-6 under 35 U.S.C. 103(a) as being unpatentable over Majos Jacques, EP1187308 in view of Yu et al., US Patent 5793096, Applicant argues "Yu does not appear to teach or suggest superimposing inductors one on top of the other. Yu appears to teach superposing an

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inductor onto transistors, which reduces the chip area since a separate area for the MOS transistors is no longer necessary. Consequently, Yu does not appear to saving more than either the inductor area or the transistors area". This argument is not persuasive because the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Applicant further argues, "The inductors of EP 1187308 doe not appear to be mutually coupled". This argument is not persuasive because "the inductors being mutually coupled" is an obvious consequence of the two spiraled inductors being superposed on top of the other. Applicant further argues that the cited art does not suggest the features in dependant claims. These limitations "the inductors are in the form of spiraled capacitors formed by metal implantation in the metallization levels that are isolated by a thin oxide film" or "wherein each inverter comprises two oppositely biased MOS transistors placed in line, the input of the inverters being located on the gate of one of the transistors having a first bias and the out at the mid-point of the two transistors" or "an amplification stage comprising two oppositely biased MOS transistors placed in series, the gate of each MOS transistor being coupled to one of the outputs of the oscillating stage". These arguments are not persuasive because Figure 2 of Majos Jacques clearly shows the features as recited in the claims as shown in Fig.1 of this instant application.

### Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph Chang Patent Examiner Art Unit 2817